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SMITH PATENT OFFICE
1901 PENNSYLVANIA AVENUE N W
SUITE 200
WASHINGTON, DC 20006

EXAMINER	
GRAHAM, ANDREW R	
ART UNIT	**PAPER NUMBER**
2644	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,912	MIYASAKA ET AL.	
	Examiner	Art Unit	
	Andrew Graham	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on August 2, 2004. These drawings are have been approved by the examiner and have been entered into the case. The previous objections to Figure 6, 12, and 17 are hereby withdrawn.

Specification

2. The changes made in regards to the word "Huffman" are acknowledged and approved. The previous relevant objection is hereby withdrawn.

3. The specification is newly objected to because of the following informality:

On page 5, line 20, the process of Figure 3 is referred to as being "parallel". However, Figure 3 appears to illustrate a serial processing of functions A and then B.

Appropriate correction or clarification is required.

4. The amendment made to the title is acknowledged and approved. The previous relevant objection is hereby withdrawn.

Claim Rejections - 35 USC § 112

5. The amendments made to Claims 9 and 18 in view of the previous rejections made under 35 U.S.C. 112 are sufficient to overcome the grounds of the previous rejections. Accordingly, said previous rejections are hereby withdrawn.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10-12, 14-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the amendment of August 2, 2004, Claim 10 presently states, "a main signal processing section. . . which completes a first process within a period T" and "first process excludes information generated in a past time frame". Claim 10 also states, "first to Nth sub signal processing sections . . . completing a second process within a period T" with second process "using the information generated in the past time frame". These limitations appear to conflict with, and are not supported by the applicant's specification, as originally filed. As a feature of a processing time requirement of N*T, which is longer than the time requirement for the main processor, the first to Nth sub signal processors are understood to be operating in parallel. It is unclear how a parallel processing stage would have been able to "use information generated in the past time frame" because such information

would have been still subject to processing in a different sub signal processing stage, and therefore unavailable to all processors.

It appears that the applicant has attempted to combine the limitations of previous Claim 13 into Claim 10. However, the "first" and "second" process are reversed in the present claim language. Accordingly, it is suggested that Claim 10 intends to recite "a main signal processing section. . . which completes a first process within a period T" and "first process using the information generated in a past time frame and "first to Nth sub signal processing sections . . . completing a second process within a period T" that "excludes information generated in the past time frame". Appropriate clarification or correction is required.

Claims 11-12 and 14-17 are rejected based on their respective dependencies upon Claim 10.

Claim 18 recites the same relationship between the main processor and first process, as well as between the Nth sub signal processors and is rejected based upon the same grounds as recited above for Claim

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1, 2, 8-11, and 17-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over by Ahamed et al (USPN 5978831).

Ahamed discloses a multiprocessor architecture that utilizes processors with different processing rates. As is generally shown in Figure 1, the teachings of Ahamed center around multiple processors connected in parallel, wherein the processing rates of the involved processors are integer multiples of each others and are less than the rate at which data is received in the processing section (col. 7, lines col. 8, lines 66-67 and col. 9, lines 1-3). The basic embodiment shown in Figure 1 uses an input gate (17), buffers (19,20), and an output gate (18) to control the transfer of data between the processors and in and out of the processing section (col. 7, lines 54-67 and col. 8, lines 1-21). With a delay between the input of a particular frame of information data and the output of the same data from the parallel processing scheme, the stage is able to obtain a constant rate of throughput equivalent to the arrival time of the blocks of information data (col. 7, lines 49-51). The delay of the system is equivalent to the execution period of the slowest processor in the system. Ahamed also discloses that the parallel processing scheme may be implemented into a pipeline wherein the individual parallel processing schemes illustrated in the disclosure are the stages of the pipeline. Ahamed discloses that the stages require the same amount of execution time so that each stage is continually busy (col. 11, lines 31-37). Ahamed provides the equations for a general

parallel arrangement for any number of (k) parallel processors, with an integer relationship between processing speeds (col. 9, lines 45-67; col. 10, lines 1-50). One such "any integer" relationship is "1". The overall system, in particular view of the generalized structure teachings, reads on "A signal processing device" and a single stage of multiple, parallel processors reads on "first to Nth sub signal processing sections each of which is given (N x t + I)th frame signals (I and t are integers, N is a natural number, and $0 \leq i \leq N$) of a first digital signal framed for each predetermined time interval". The execution periods of the multiple processors in parallel reads on "completes a first process within a period (N x T)" (col. 10, lines 24-45). The nature of the parallel processing does not allow processing relationships between sequences of input frames, as input frames are allocated to different processors. For example, process ID3 in Figure 2 cannot require the output of process ID0 because, at the initial time of processing of ID3, the result of ID0 has not been obtained. This reads on "the first process excludes the information generated in the past time frame".

Again, while Ahamed discloses the arrangement of stages of processing in a pipeline, Ahamed does not explicitly teach:

- a main, single processor for performing a function in the processing scheme
- that the single processor completes a process within a period T

However, Ahamed specifically discloses that the multiprocessor stages have an equal functional performance capability to that of a single processor, an equivalence which suggests interchangeability (col. 2, lines 47-52). Regarding Figure 14, Ahamed also notes that any arbitrary segment of the shown pipeline may be replaced by a series processor arrangement, which also suggests the use of a processor with a single input and output as part of the pipelined system (col. 11, lines 51-54 and col. 12, lines 25-28). A single processor though which all signals pass is the fundamental serial processing arrangement. This form of processing, in view of any arbitrary segment such as the middle or later pipeline stages (1402-1404) reads on "a main signal processing section which converts a signal processed in said (i+1)th sub signal processing section into a second digital signal". Again, Ahamed discloses that each stage of the pipeline would need the same execution time (col. 11, lines 31-37). Ahamed teaches the use of a multiprocessor stage in a multistage pipeline as an option or alternative, which allows for use of such a serial or single processor for a stage not implemented in multiprocessor, varying rate manner (col. 11, lines 29-31). A single processor serving as a stage in such a pipeline inherently requires an execution time of less than that of the multiple processors in parallel by virtue of having the same throughput. This aspect of the teachings of Ahamed reads on "completing a second process within a period T". The sequential nature of a pipeline requires any stage that follows another stage to employ previously processed data. For

the serial or unbranched arrangement discussed above, in view of stages (1402-1404) of Figure 14, this reads on "contains a process employing information generated in a past time frame".

It is further noted that an actual length of time for period T is not required by the claims other than that N processors be able to complete a process within a period N*T, and a main processor complete a processor within a period T. While these limitations put a minimum length on the interpretation of T, they do not designate a maximum length for an interpretation of the length of a period T.

It is also further noted that t is not further delimited, beyond the requirement that it is an integer.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to include a single processor as a stage of the pipelined processor architecture of the invention of Ahamed. The motivation behind such a modification would have been the lower price, in certain situations, of using a single processor instead of several, as suggested by Ahamed. The use of a single processor in a pipeline stage would have also provided the benefits of simpler input, output, and power connections for the particular stage, a reduced physical area required for the stage, as opposed to the potential multiple clock cycles needed to be addressed in the multiprocessor stages. Ahamed states that very fast chips, though more rare, are still yielded by manufacturers; implementing them as proposed above would have provided use, when afforded by the processing speed of the processor, for implementing both very fast and

not as fast processors in the same system, while not requiring the additional production of either particular speed of processor.

Regarding **Claim 2**, the input gate (17) and the input buffer (19) of the first shown embodiment deliver the appropriate blocks of input signal to the appropriate signal processors (col. 7, lines 64-67 and col. 8, lines 1-8). The delivery timing of said input gating component (17) can be seen in Figure 2. These components read on "a distribution section inputting said first digital signal to one of said first to Nth sub signal processing sections for each time frame interval one after another". The output gate (18) outputs the data block in the order of their input (col. 8, lines 8-15). Ahamed also notes that the output gate of one stage may be the input gate of another stage (col. 12, lines 59-62). This output gate (18) reads on "a selection section selectively outputting one of the after-process signal outputted from said first to Nth sub signal processing sections for each frame interval one after another to input the signal to said main signal processing section".

Regarding **Claim 8**, Ahamed discloses the use of m parallel processors with any integer relationship between the processing rates of the involved processors (col. 9, lines 1-3). Ahamed particularly teaches the fractional relationship between processors (col. 10, lines 14-50). As note above, the integer of "1" is one such integer relationship clock that may be applied to the generalized teachings of Ahamed (col. 9, lines 45-48). Ahamed, again, also discloses that each stage of a pipeline is given that same processing time, and thus,

where a single processor makes up a stage of the pipeline, the processing time allowed for the single processor is t (col. 11, lines 31-37). These relationships in view of the possible combinations of processors of Ahamed read on "division is made for said first process and said second process so that the calculation period necessary for said first process is N times the calculation period necessary for said second process".

Regarding **Claim 9**, please refer to the like teachings of Claim 1. Regarding **Claim 10**, please refer to the like teachings of Claim 1, , again noting that Ahamed teaches the use of a serial arrangement for any segment of such a network, as well as the associated properties of parallel and serial processing. Regarding **Claim 11**, please refer to the like teachings of Claim 2. Regarding **Claim 17**, please refer to the like teachings of Claim 8. Regarding **Claim 18**, please refer to the like teachings of Claim 1 and 10.

8. **Claims 3 and 12** are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ahamed as applied above, and in further view of Matt et al (USPN 6581153). Hereafter, "Matt et al" will simply be referred to as "Matt".

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed also discloses the components necessary for properly transferring the data between the processor or processors that make up each stage of the pipeline, including those that act as both the

output for one stage and the input for the next stage. Ahamed discloses the concept of stages of the pipeline having input and output buffers (col. 8, lines 1-15). Ahamed also discloses the use of Input/Output (I/O) buffering, which involves the handling and temporary storing of pre- and post-processed data (col. 6, lines 23-27). These teachings, in view of the processing performed on the respective signals, reads on "a first memory storing said frame signal one after another" and "a second memory storing said frame signal of said second digital signal one after another". Ahamed also discloses the use of a memory and a single control unit for an embodiment of the disclosed systems.

While Ahamed discloses different components for the distribution and selection of the data being received and transferred from the processors in the system, Ahamed does not specify:

- a distribution and selection for controlling data transfer between processing sections
- the connection of a main signal processing section to the two memories, including the respective data transfers between the memories and the main processor

Matt discloses a central router component that handles the transfer of data between a main, single processor and a plurality of individual, function specific processing modules. The router (ROUTER) specifically coordinates the relaying of data between the processing modules (M1,M2,M3) and the main processor (DSP), as well as between the processors and a memory (RAM) (col. 4, lines 13-29). The data for

the modules is transferred from the DSP, and the processed data is then transferred back to the DSP. The RAM can be used to store data before processing by the modules as well as storing data before it's transferred back to the DSP (col. 4, lines 24-52 and col. 6, lines 47-51). The router and its application reads on "a distribution and selection section" and "wherein said first to Nth sub signal processing sections are connected to said distribution and selection section" and "sends the after process signal to said distribution and selection section". The connection of the DSP to input and output paths as seen in Figure 1, in view of the I/O buffering and control disclosed by Ahamed, reads on "said main signal processing section is connected to said first and second memories" and "picks out said frame signal from said first memory for each time interval T to output said frame signal to said distribution and selection section" and the other relative connections between the memories and the DSP.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the central router of Matt to distribute the data between the processing stages of the system of Ahamed. The motivation behind such a modification would have been that the central router would have retained computing capacity for a main processor. In view of the teachings of Ahamed, the central data router of Matt would have also enabled data to flexibly transferred between modules.

Regarding **Claim 12**, please refer to the like teachings of Claim 3.

9. **Claims 5-7 and 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahamed as applied above, and in further view of the applicant's admitted prior art.

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed also notes the general concept of having different processors with different functionalities incorporated into the same system (col. 4, lines 48-64). The processing blocks are suggestedly separated according to function, but organized sequentially according to processing time (col. 4, lines 60-64).

Ahamed does not disclose particular further details about the functions performed by the different stages of the presented pipeline arrangement, including:

- that the first digital signal is a compressed and encoded signal
- that the second digital signal is a pulse code modulated signal of an audio signal
- that the first process involves converting the information in the data into the frequency spectrum
- that the second process converts the frequency spectrum signal into a time based pulse code modulated signal

However, the applicant has noted that a number of types of compressing/decoding process techniques are known in the art (page 1,

lines 9-15 of the submitted specification). Listed processes include subband encoding, MDCT, quantization, and Huffman encoding, as well as the compression technique of MPEG-1 Layer 3. The MPEG-1 Layer 3 encoders are known in the art to include each of these four processes. The Pohlmann reference has been included with this action to provide support for such a position. Figure 11-20-B of Pohlmann clearly illustrates the conversion of an encoded audio bitstream to a stereophonic digital audio signal with an MPEG-1 Layer 3 decoder. In view of this decoding process, as cited as known in the art by applicant, the input signal to the decoder reads on "said first digital signal is a compressed and encoded signal of an audio signal". The output signal of the MPEG-1 Layer 3 decoder reads on "said second digital signal is a PCM signal of an audio signal". The Huffman decoding and bit reallocation of an MPEG-1 Layer 3 decoder reads on "contains a process picking out information from the compressed and encoded signal to convert the information into information of a frequency spectrum". The inverse MDCT procedure and inverse subband filtering of a MPEG-1 Layer 3 decoder reads on "contains a process converting said information of said frequency spectrum into said PCM signal of time base".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the processing architecture of Ahamed to perform the audio encoding and decoding processes noted in the applicant's admitted prior art. The motivation behind such a modification would have been a throughput rate

equivalent to the input rate that the system of Ahamed that would have provided for the processes of audio encoding and decoding, processes which heavily rely on the timely presentation and execution of data. Ahamed also discloses that the parallel processing scheme is, in certain instances, more cost effective than a single processor.

Regarding **Claim 6**, the applicant discloses Huffman coding and MDCT as well-known processes in the art. The MPEG-1 Layer 3 decoder and other digital decompression/decoding techniques are well known in the art to include both a Huffman decoder and an inverse MDCT, which reads on "said first process contains a decoding process of a variable length code" and "said second process contains an inverse MDCT process".

Regarding **Claim 7**, the applicant discloses quantization and subband encoding as well-known processes in the art. The MPEG-1 Layer 3 decoder and other digital decompression/decoding techniques are well known in the art to include both an inverse quantizers and sub-band filters, which reads on "said first process contains an inverse quantizing process" and "said second process contains a sub-band synthesis filter bank process".

Regarding **Claim 14**, please refer to the like teachings of Claim 5. Regarding **Claim 15**, please refer to the like teachings of Claim 6. Regarding **Claim 16**, please refer to the like teachings of Claim 7.

10. **Claims 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahamed as applied above, and in further view of Buchheim (USPN 6061306).

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed's disclosure focuses on the architecture of the involved processors, not necessarily the large scale device in which said teachings may be implemented. In terms of processing though, please refer to Claim 1 regarding Ahamed's teachings and the "first to Nth sub signal processing sections" and "main signal processing section" in Claim 19.

Ahamed does not specify:

- that the overall device is a portable type apparatus including:
  - an audio signal input section for inputting an encoded audio signal
  - a signal processing device for decoding said audio signal through the use of sub signal processing sections and a main signal processing section

Buchheim discloses a digital music player that is capable of conducting various forms of input and output. The overall player, as shown in Figure 2, the overall device is implemented in a housing shaped like and is the same size as a standard audio cassette, which means that the overall device reads on "A portable type apparatus". The device is able to output a signal through a standard audio

cassette player, built-in speakers, or external speakers (col. 6, lines 1-21). These output paths and devices read on "an audio signal output section for outputting said decoded audio signal". The device is able to receive various, compressed digital audio files through a communicator (34) which connects the device to a computer (36) (col. 7, lines 1-35). This communicator (34) reads on "an audio signal input section for inputting an encoded audio signal". The device also includes an audio chip for encoding and decoding a variety of file formats, which reads on "a signal processing device for decoding said encoded audio signal" (col. 5, lines 42-51).

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to implement the processing scheme of Ahamed into the portable digital audio player of Buchheim. The motivation behind such a modification would have been that the processing structure of Ahamed would have enabled different processing stages to be implemented in the player at a lower price than a single processor, without a decrease in the throughput of the system.

Regarding **Claim 20**, please refer to the like teachings of Claims 1, 2, and 19, noting that the microphone input ports and encoding capabilities of the device of Buchheim, as well as the memory (16) included in the portable audio player (col. 5, lines 54-56 of Buchheim).

Response to Arguments

11. Applicant's arguments filed on August 2, with respect to the previous application of the reference of Hall, Jr, and the new limitations of the relevant claims, have been fully considered and are persuasive. The rejection of Claims 1-2, 9-11, and 18 in view of Hall has been withdrawn.

Applicant's arguments filed August 2, 2004 in regards to the application of the reference of Ahamed et al (USPN 5978831) and other references under 35 U.S.C. 103(a) have been fully considered but they are not persuasive.

On page 45, lines 1-5, the applicants have stated, "Ahamed et al. do not disclose that a main signal processing section which converts a signal processed in a (i + 1)th sub signal processing section into a second digital signal by completing a second process within a period T as recited in claims 1, 19 and 20". The examiner respectfully disagrees. Ahamed teaches that pipeline architectures comprises stages of processing, wherein each stage needs the same amount of finite time for execution (col. 11, lines 24-34). Ahamed teaches that the multiprocessor structures disclosed therein can be applied to any such stages, in contrast with each of such stages, which allows for the multiprocessor structures to not be applied to a stage. Ahamed then emphasizes that any arbitrary segment of such a network may be replaced by a series processor (col. 11, lines 51-54). A fundamental series arrangement comprises a single processor that handles all

inputs and outputs in a particular part of the processing. A basic, arbitrary segment of the network, as permitted by Ahamed includes a single stage in a processing arrangement, such as the final stage (404) of Figure 13.

The concept of a period "T" relates to the uniform completion time for stages of processors, as is disclosed by Ahamed. "T" is undefined in the claims, enabling its interpretation to be arbitrary, though reasonable, with the only requirement being that a processing time of N processors in a prior stage be completed within T*N and a single processor be completed within T. As noted above, this does not put a maximum on the valid interpretation of T. However, Ahamed teaches that each stage of a pipeline architecture has the same throughput. Ahamed also teaches that the multiple parallel processors may have the same throughput as the input. As such, a uniprocessor stage, though not mandated but also not excluded from the possible implementations of stages of the pipeline, would be required to also operate at the throughput rate. These collective teachings of Ahamed read on "complete a second process within a period T" as included in the claim.

The motivation behind substituting a single stage in such a pipeline network, as presented in the previous and current office action, would have centered around the simplicity of various connections of such an arrangement, as would have been recognized by one of ordinary skill in the art by virtue of the use of a single processor. Such a stage would have eliminated the need for input and

output data routers, such as the multiple input and output gates depicted in Figure 4. It is in view of the replacement of arbitrary segment with a series processor, as is disclosed by Ahamed that such a limitation is considered obvious, with the benefits of single chip processing providing desirability or motivation for such a substitution. Ahamed also teaches that not all situations involve a cheaper use of a plurality of processors instead of a single, higher rate processor.

On page 45, lines 5-9, the applicant has stated, "Ahamed et al. also do not disclose that the second process contains a process employing information generated in a past frame time; and the first process excludes the information generated in the past frame time as recited in claim 1". The examiner respectfully disagrees. As cited above, Ahamed teaches that any arbitrary segment of a computer network may be replaced by a series, parallel, or series/parallel segment (col. 11, lines 51-54). Ahamed also discloses a pipeline architecture for processing in Figure 13 (col. 11, lines 24-28). Applying the former statement to the latter, a stage comprising parallel computing that is sequentially followed by a stage that comprises serial computing is one subcombination of the teachings of Ahamed. Parallel stages cannot involve data that relies upon data processed in a previous frame, as an inherent aspect of such concurrent processing. A series stage that follows such a stage must rely on the output frame of the previous stage because, by definition of a series computation, data is processed in the stage sequentially. Thus, a first process

not depending on a previous frame and a second process that follows the first process and depends on a previous frame is an inherent aspect of one combination of processing arrangements taught by Ahamed. This response, as well of that of the above paragraphs also applied to the arguments presented on page 45 in regards to Claim 9.

In regards to the argument presented in view of Claims 10 and 18 on page 45, lines 19-22 and page 46, lines 5-9, it is respectfully submitted that such grounds are not supported by the applicant's disclosure, as detailed above in regards to the rejection of Claims 10-12 and 14-18 under the first paragraph of U.S.C. 112.

On the last line of page 45 and page 46, lines 1-5, the applicant has stated, "Ahamed et also do not disclose that a main signal processing section which is given (N*t+I) frame signals and t are integers, N is a natural number, 0<= i < N) of a first digital signal framed for each predetermined time interval and which completes a first process within a period T (T is a real number) as recited in claim 10". The examiner respectfully disagrees. Similar to above, Ahamed teaches that any arbitrary segment of a computer network may be replaced by a series, parallel, or series/parallel segment (col. 11, lines 51-54). Ahamed also discloses a pipeline architecture for processing in Figure 13 (col. 11, lines 24-28). Applying the former statement to the latter, a stage comprising serial computing that is sequentially followed by a stage that comprises parallel computing is one combination of the statements of Ahamed. A series stage that must rely on the pipeline input frame or output frame of the previous stage

because, by definition of a serial computation, that data is processed in the stages sequentially. A parallel stage that follows such a stage cannot involve data that relies upon data processed in a previous frame, as such data is simultaneously being handled by a different branch of such processing, as is generally illustrated in Figure 2 of Ahamed. Thus, a first process depending on a previous frame and a second process that follows the first process and does not depend on a previous frame are inherent aspects of combinations of processing arrangements taught by Ahamed.

Again, the concept of a period "T" relates to the uniform completion time for stages of processors, as is disclosed by Ahamed. "T" is undefined in the claims, enabling its interpretation to be arbitrary, though reasonable, with the only requirement being that a processing time of N processors in a prior stage be completed within T*N and a single processor be completed within T. As noted above, this does not put a maximum on the valid interpretation of T. However, Ahamed teaches that each stage of a pipeline architecture has the same throughput. Ahamed also teaches that the multiple parallel processors may have the same throughput as the input. As such, a uniprocessor stage, though not needed but also not excluded from the possible implementations of stages of the pipeline, would be required to also operate at the throughput rate. These collective teachings of Ahamed read on "complete a first process within a period T" as included in the claim.

On page 46, lines 10-15, the applicant has stated, "Ahamed et al. also do not disclose that converting a (N + 1)th frame signal processed by said main signal processing section and given to said first to Nth sub signal processing sections one after another, into said second digital signal by completing a second process within a period (N x T) in the first to Nth sub signal processing sections as recited in claim 18". The examiner respectfully disagrees. Please refer to the above discussion regarding Ahamed's disclosure that any arbitrary segment of a computing network may be serial or parallel, particularly in the context of the single input/single output stages illustrated in Figure 14. The output of each stage, in the system of Ahamed, is presented and processed in a sequential manner that reflects the order of signal input. Ahamed discloses that processors process blocks of data in the same duration of T seconds proportionate to their processing speeds, wherein the processing speeds are related by an integer or fraction (col. 9, lines 44-67; col. 10, lines 1-50). Ahamed specifically teaches that the period T = N*t, wherein N is related to the proportionate processing speeds per parallel processor and t is in seconds, the data arriving uniformly in one block per second. Figure 10 illustrates a generalized structure enabling use of an integer relationship between processing speeds (col. 9, lines 10 and 45-48). Again, the maximum limit of T is not specified, neither are minimum, maximum, or any ongoing relationships for the variable t.

On page 46, lines 16-18, the applicant has stated, "Ahamed et al. does not teach or suggest the usage of a pipelined multi-processor and

the replaced single processor". The examiner respectfully disagrees. Ahamed teaches that any arbitrary segment of a computer network may be replaced by a series, parallel, or series/parallel segment (col. 11, lines 51-54). Ahamed also discloses a pipeline architecture for processing in Figure 13 (col. 11, lines 24-28). Applying the former statement to the latter, a stage comprising parallel computing that is sequentially followed by a stage that comprises serial computing is one combination of the architecture disclosed by Ahamed. A series arrangement comprises at least a single processor that handles all of the inputs for the corresponding or prescribed stage of processing. Figure 1 of Ahamed illustrates that parallel processing comprises at least two processors in separate branches through which data flow. Stages of a pipelined architecture are included in the definition of "any arbitrary segment of a computing network". In reference to this pipeline Ahamed teaches that the multiprocessor stage may be included in any stage of the architecture, in contrast to each stage, which suggests that single processor stages are being replaced by multiple processor stages (col. 11, lines 29-31).

On page 47, lines 1-3, the applicant has stated, "one of ordinary skill in the art would not have combined these references to render the claimed invention obvious" and "there is no teaching or suggestion for the combinations in the applied proposed references". The examiner respectfully disagrees. In summary, the motivation behind the teachings of Ahamed relies upon the benefits of being able to utilize a single processor to meet the requirements of a pipeline stage. The

use of a high speed processor is noted as not always more expensive than the use of plural, single processors. Ahamed teaches the use of parallel processing as an option for stages in a pipeline architecture. Ahamed teaches that manufacturers produce processors of different speeds; thus, a single processor that meets the throughput requirement of a connected pipeline stage would provide the necessary processing speed without the need to produce or connect another microprocessor. The teachings of Matt would have enabled a separate processor to selectively route data between processors, as opposed to a hardwired configuration suggested by Ahamed, while centrally and simultaneously controlling the overall processes and retaining computing capacity for a main processor. Such a selective configuration would have enabled reconfigurable or flexible data routing. The functions of the applicant's admitted prior art are known operations with known sequential executions; the system of Ahamed would have enabled the processes to be performed at a throughput equal to the data input rate, which would have been particularly desirable in the context of audio signal processing. The reference of Buchheim applied to Claims 19 and 20 would have provided an implementation of the audio player, a consumer product, to benefit from the use of multiple processors at arbitrary operating speeds, as opposed to requiring complex control or only identical processors at high cost, as is disclosed by Ahamed.

In view of the above response, the above rejections of Claims 1-3, 5-12, and 14-20 have been reviewed and are respectfully maintained.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Keng et al (USPN 5883671) teaches the use of plural, parallel decoders, which output sequential data to a post processing components and individually operate at a speed less than the overall throughput speed of the system.

Numata (USPN 6363176) discloses the use of plural, parallel decoding and dequantization modules and a single inverse transform component.

Yoshida (USPN 6009205) discloses the use of two microprocessors for parallel execution of complex parts of a decompression processes, but a single microprocessor for a simple part of the decompression process.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the

statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Graham whose telephone number is (703) 308-6729. The examiner can normally be reached on Monday-Friday (8:30-5:00). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huyen Le, can be reached at (703) 305-4844. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HUYEN LE
PRIMARY EXAMINER

Andrew Graham
Examiner
A.U. 2644

ag
January 10, 2005